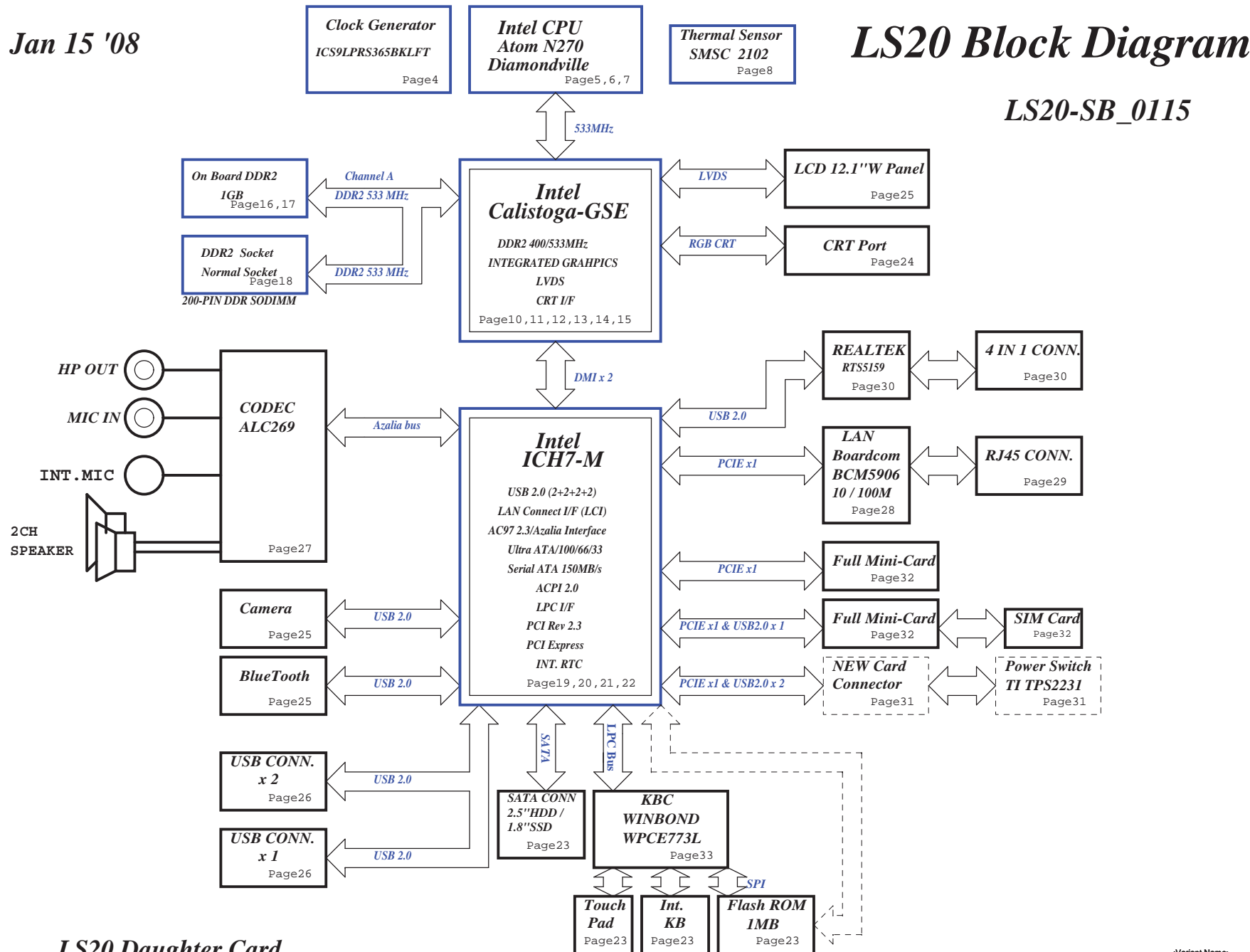


Jan 15 '08

LS20 Block Diagram

LS20-SB_0115



PCB Layer Stackup	
L1:	Signal 1
L2:	VCC
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	Signal 4

System DC/DC ISL62392	
INPUTS	OUTPUTS
DCBATOUT_62392	5V_S5 3D3V_S5
Battery Charger/Selector BQ24705	
DCBATOUT	BT+
CPU DC/DC ISL6261A	
DCBATOUT_6261A	VCC_CORE
SYSTEM DC / DC NX2139A	
DCBATOUT_2139A	ID8V_S3
SYSTEM DC / DC TPS51117	
DCBATOUT_51117_ID05V	ID05V_S0
SYSTEM DC / DC NX2139A	
DCBATOUT_2139A	ID5V_S0

<Variant Name>

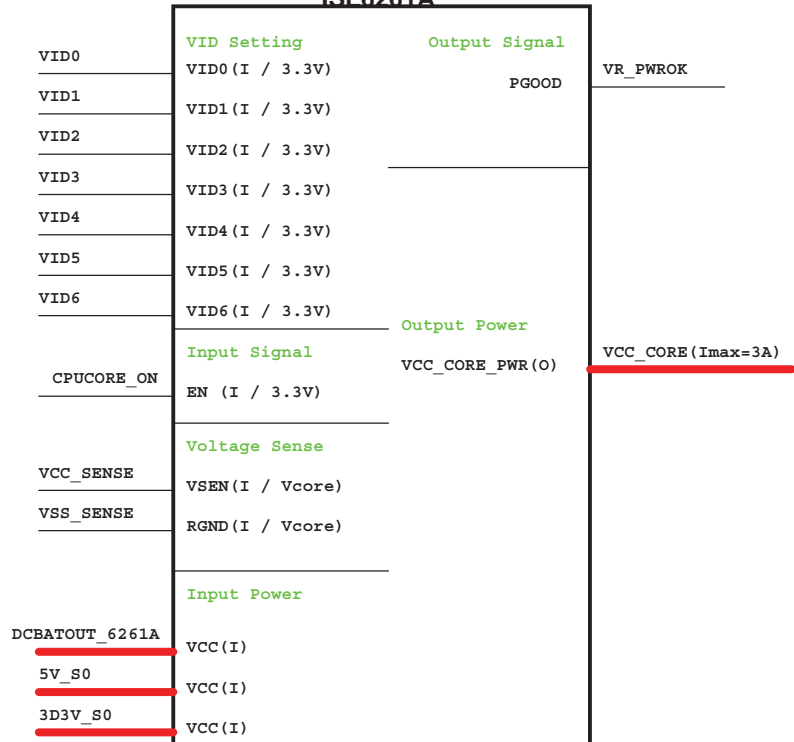
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

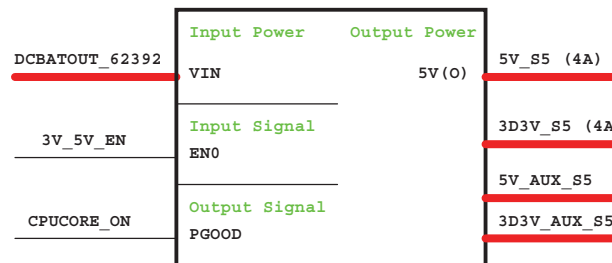
Size: A3 Document Number: **LS20** Rev: **SB**

Date: Thursday, January 15, 2009 Sheet: 1 of 41

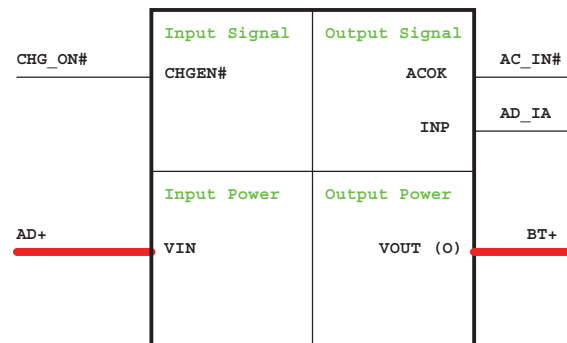
CPU_CORE ISL6261A



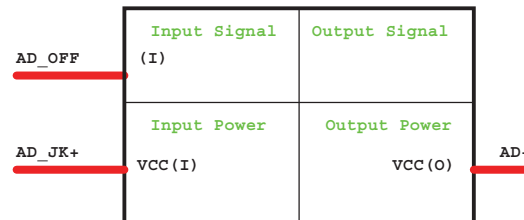
ISL62392 5V/3D3V



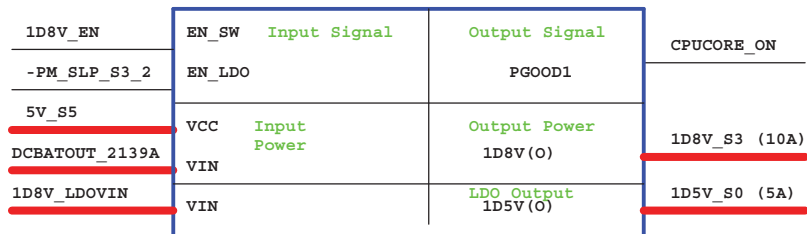
Charger BQ24705



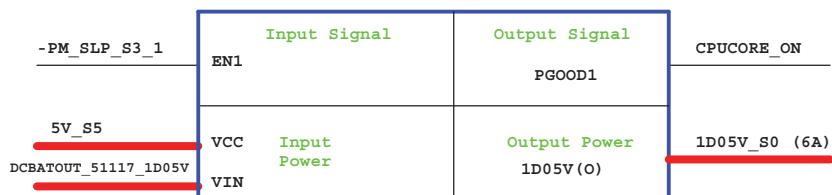
Adapter



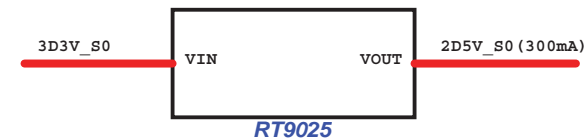
NX2139A for 1D8V and 1D5V.



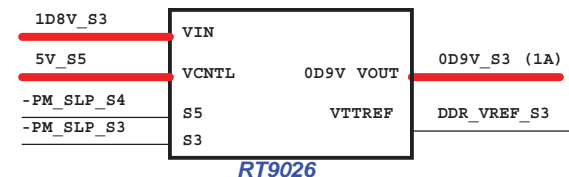
TPS51117 for 1D05V .



2D5V_S0



DDR_OD9V



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Title			
Power Sequence Logic			
Size	Document Number	Rev	SB
A3	LS20		
Date:	Thursday, January 15, 2009	Sheet	2 of 41

On Board DDR2_ID[2..0]

KBC GPIIn	47	31	23		
DDR2_IDn	2	1	0	Vendor Part No.	Size
HYNIX	0	0	0	H5PS1G83EFR-Y5C	1G
NANYA	0	0	1	NT5TU128M8DE-3C	1G
MICRON	0	1	0	MT47H128M8HQ-3:G	1G
	0	1	1		
	1	0	0		

PLANAR_ID[2..0]

KBC GPIIn		96	95	94	Planar ID Version	Planar PCB Version
PLANAR_IDn		2	1	0		
		0	0	0	LS20 Intel-SA	SA
		0	0	1	LS20 Intel-SB	SB
		0	1	0		SC
		0	1	1		-1
		1	0	0		

7,35 VCC_CORE    VCC_CORE

4,8,12,13,18,19,20,21,22,23,24,25,27,28,30,31,32,33,35,36,37,38,40,41 3D3V_S0    3D3V_S0

4 3D3V_S0_CK505    3D3V_S0_CK505

4 1D5V_S0_CLKIO    1D5V_S0_CLKIO

11,13,16,18,37,38,40 1D8V_S3    1D8V_S3

11,16,18,38 DDR2_VREF_S3    DDR2_VREF_S3

4,7,12,13,19,22,31,32,37,41 1D5V_S0    1D5V_S0

4,5,6,7,9,10,13,14,20,22,38,40 1D05V_S0    1D05V_S0

<Variant Name>

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Title

Reference

Size
A4

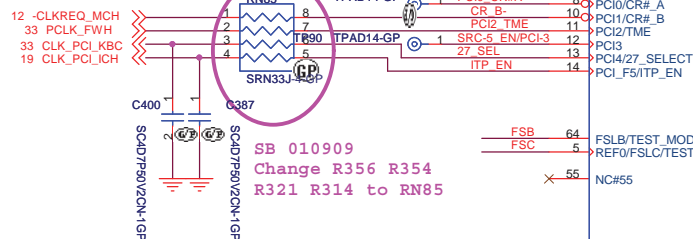
Document Number

LS20

Rev
SB

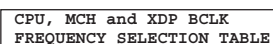
Date: Thursday, January 15, 2009

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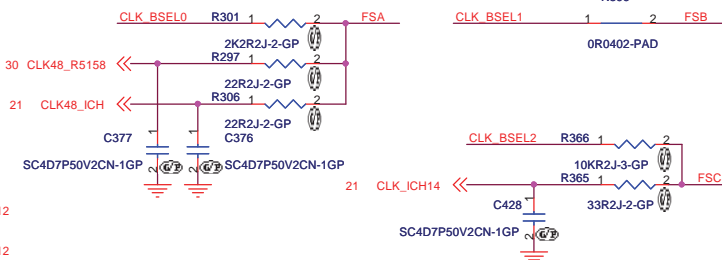
0	Overclocking of CPU and SRC Allowed
1	Overclocking of CPU and SRC NOT allowed

ITP_EN	PIN53,54
0	SRC8
1	CPU_ITP



FSC BSEL2	FSB BSEL1	FSA BSEL0	Host Clock frequency MHz
1	0	1	100
0	0	1	133
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved

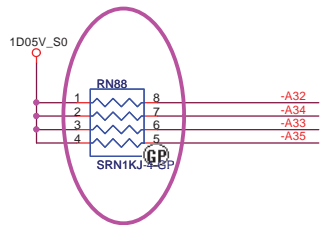
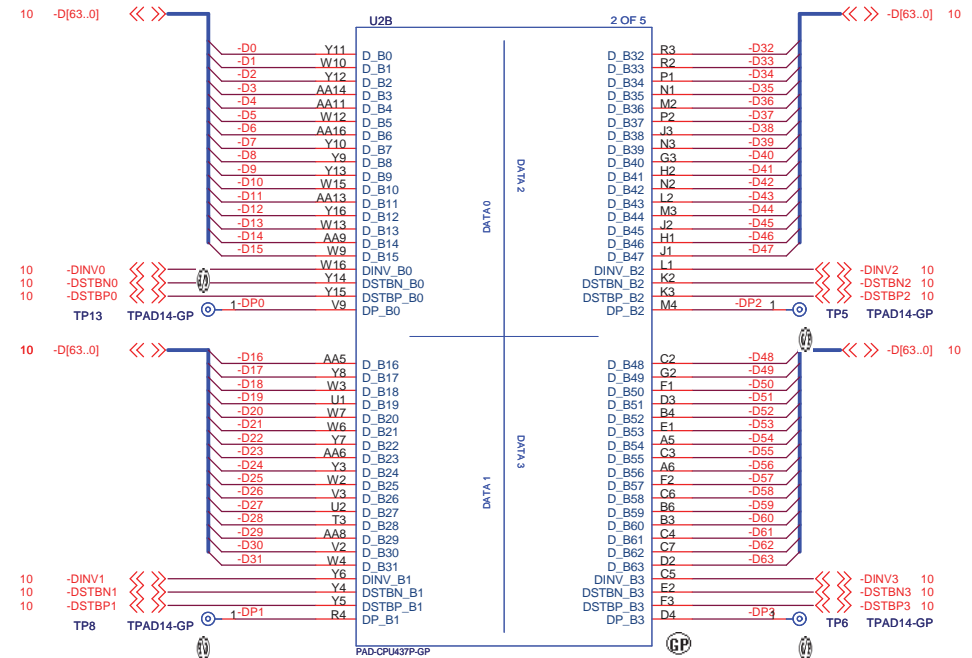
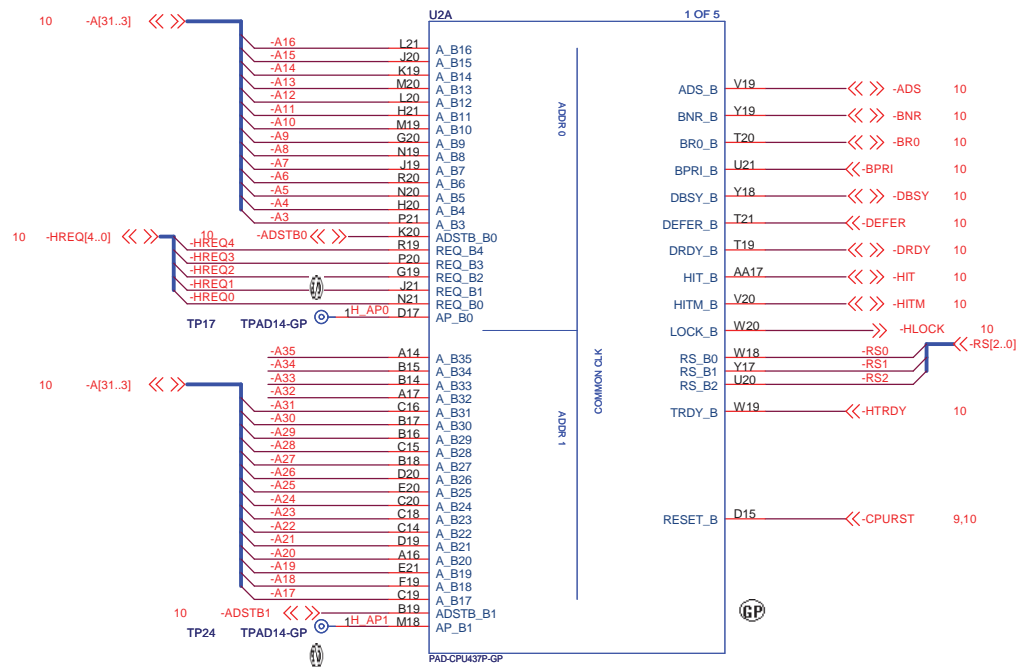
27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96	DOT96#	SRC1	SRC1#
1	SRC0	SRC0	27M_NSS	27M_SS



<Variant Name>

緯創資通 **Wistron Corporation**
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Title			
CLOCK GEN(ICS)			
Size A3	Document Number	Rev	SE
	LS20		
Date: Thursday, January 15, 2009	Sheet 4	of	41



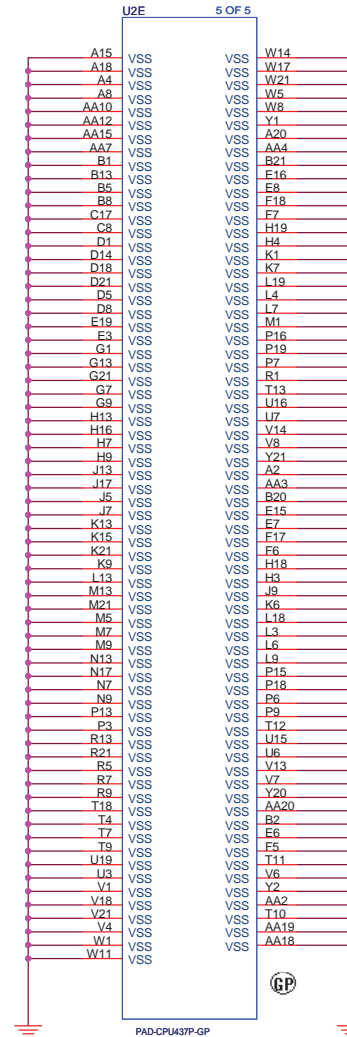
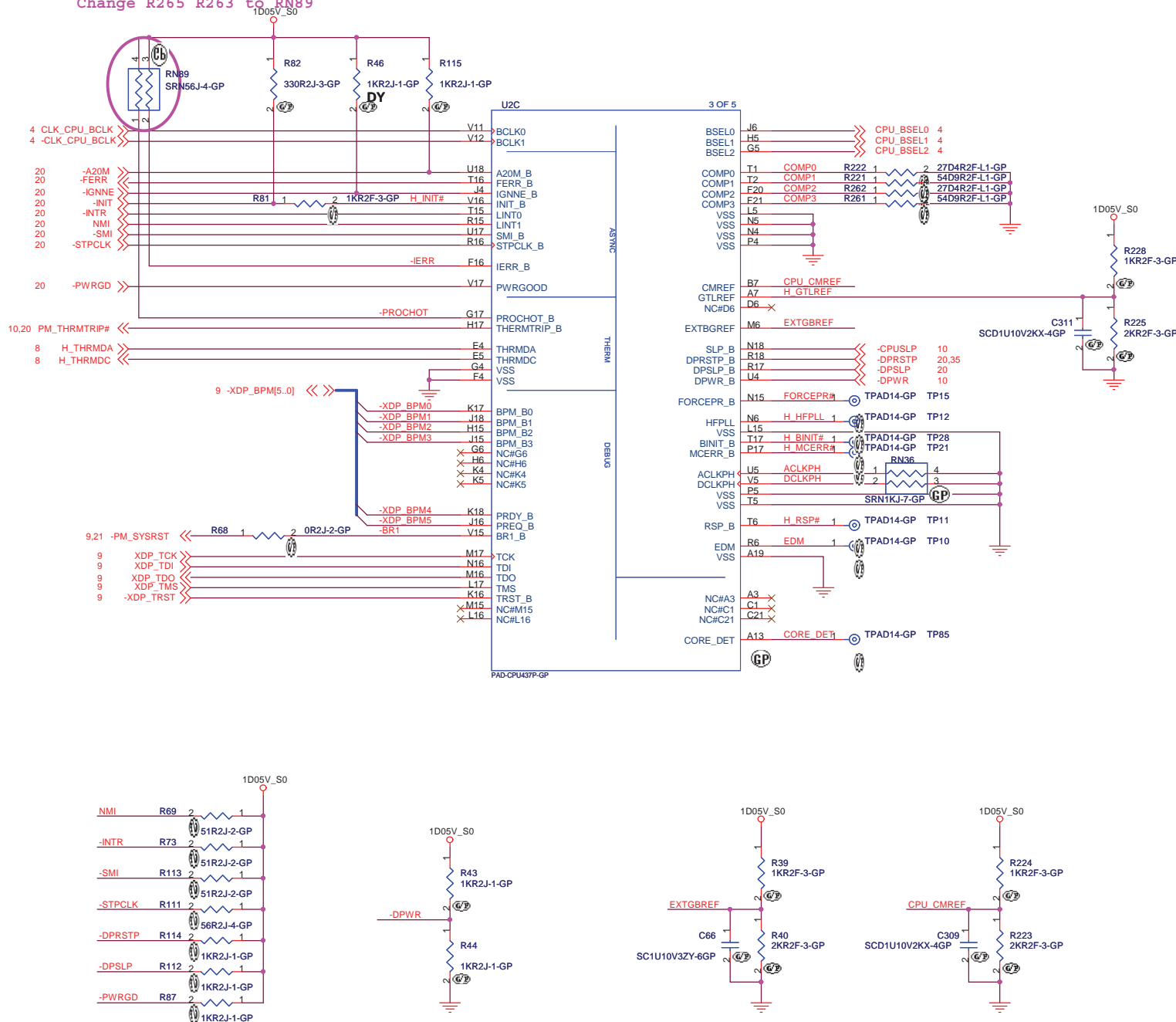
SB011009
Change R256 R253 R254 R251 to RN88
SB011309
Swap RN88 pin6 and pin7

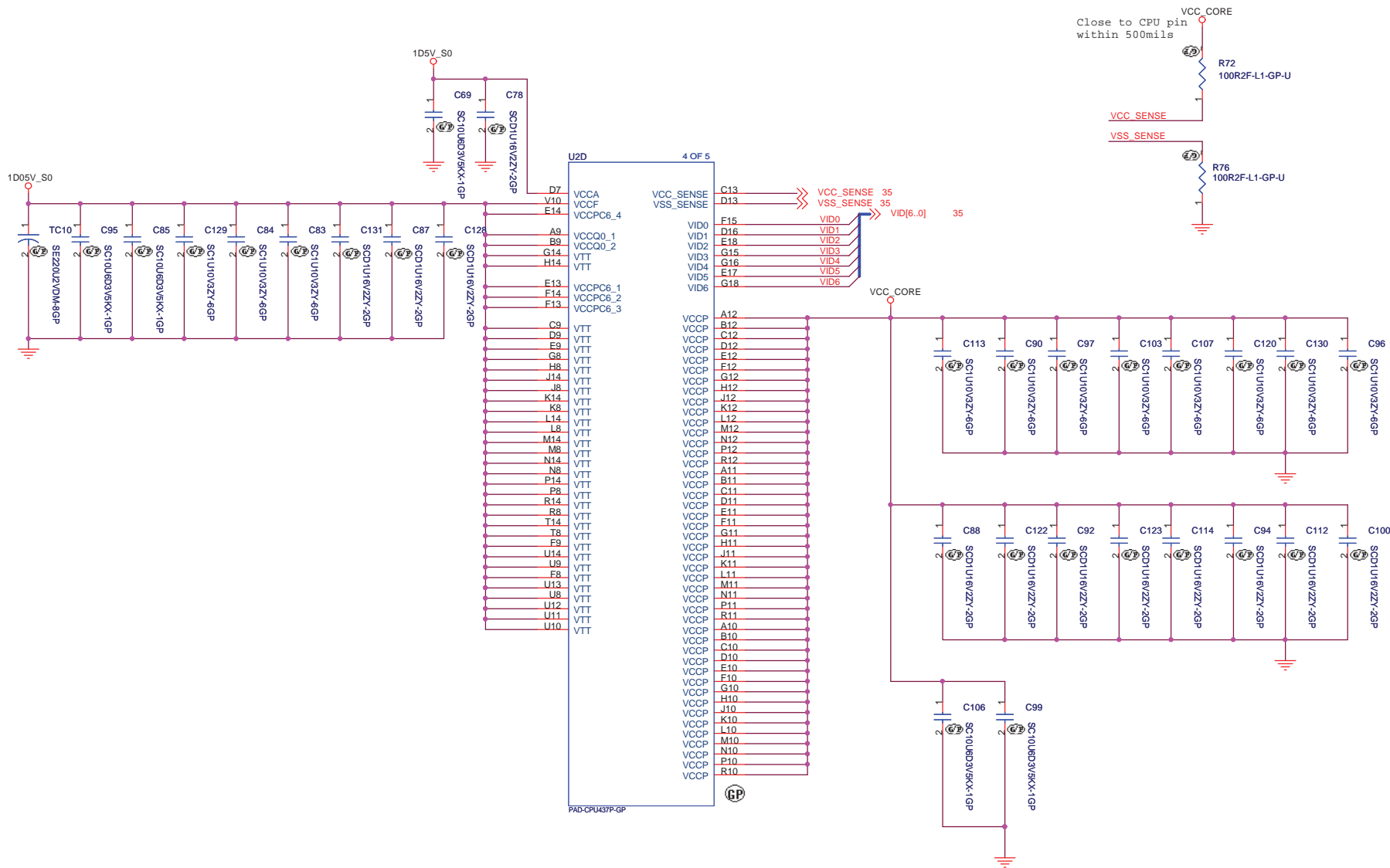
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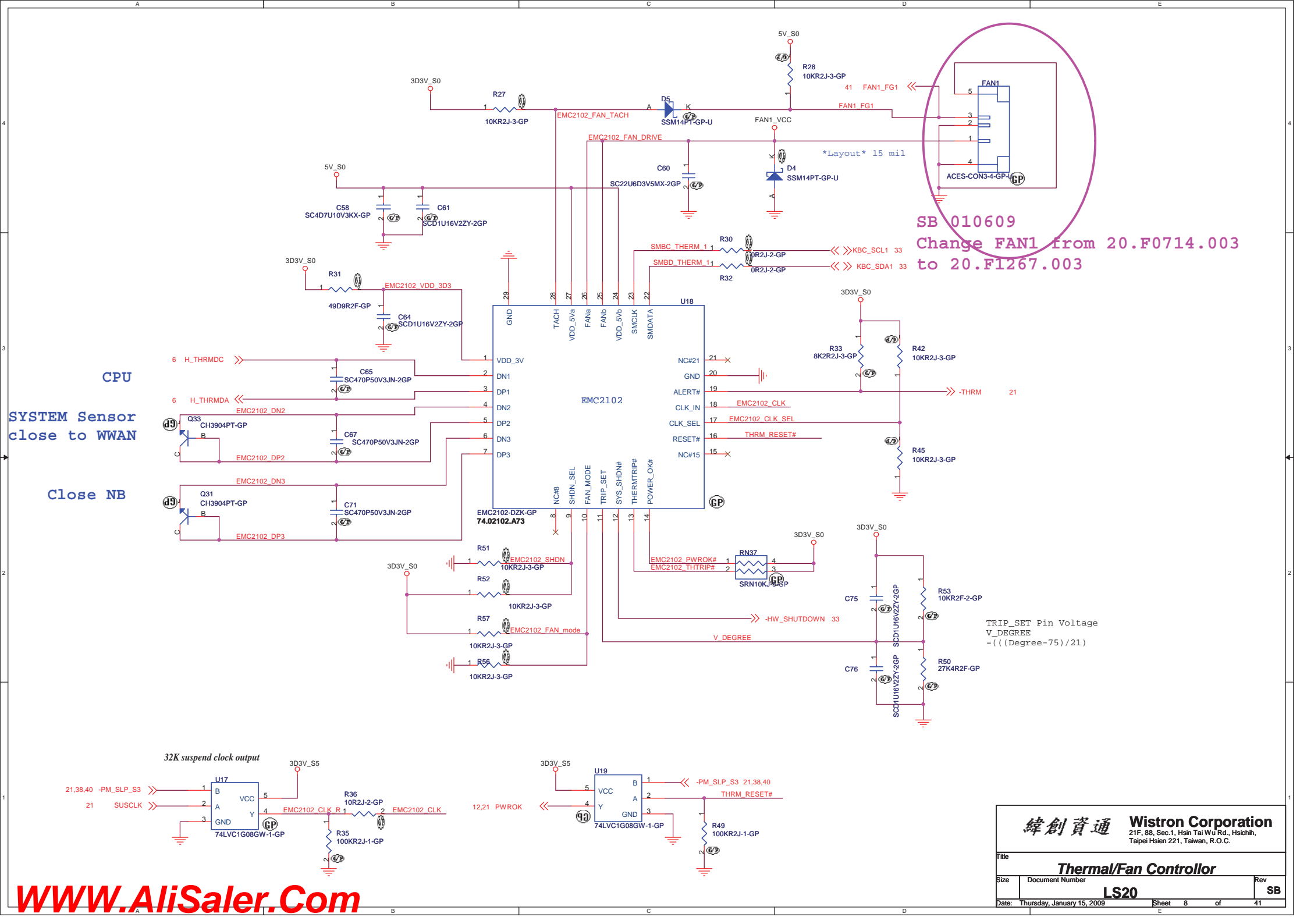
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			Diamondville CPU(1/3)		
Size	Document Number	LS20			Rev
A3					SB
Date:	Thursday, January 15, 2009	Sheet	5	of	41

SB011009
Change R265 R263 to RN89

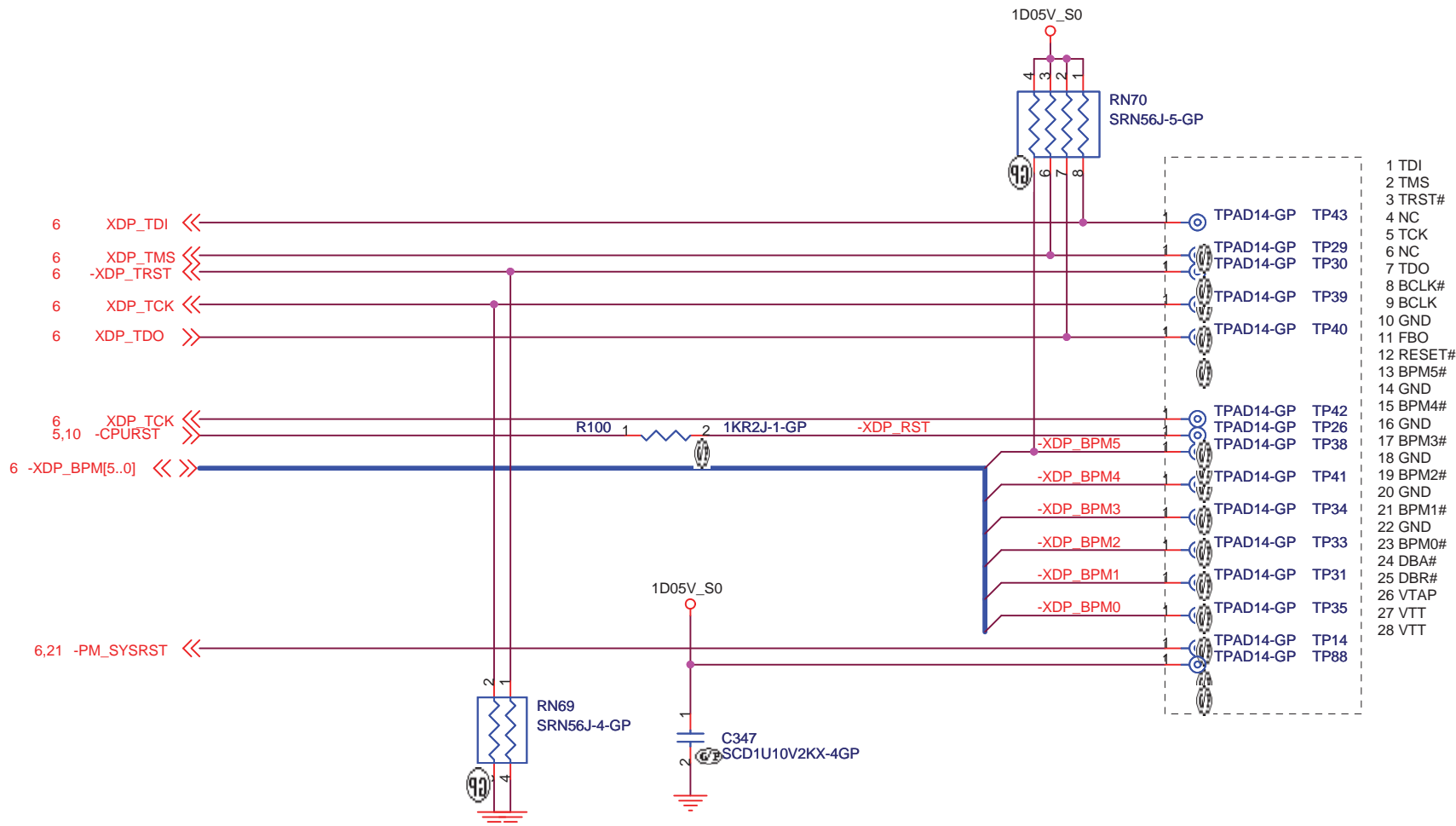






SB 010609
Change FAN1 from 20.F0714.003
to 20.F1267.003

TRIP_SET Pin Voltage
V_DEGREE
= (((Degree-75)/21))



(*1) TCK SIGNAL IS BRANCHED AT CPU's PIN

(*2) CPURST# SIGNAL IS BRANCHED AT GMCH's PIN

<Variant Name>

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Title

ITP port

Size
A4

Document Number

LS20

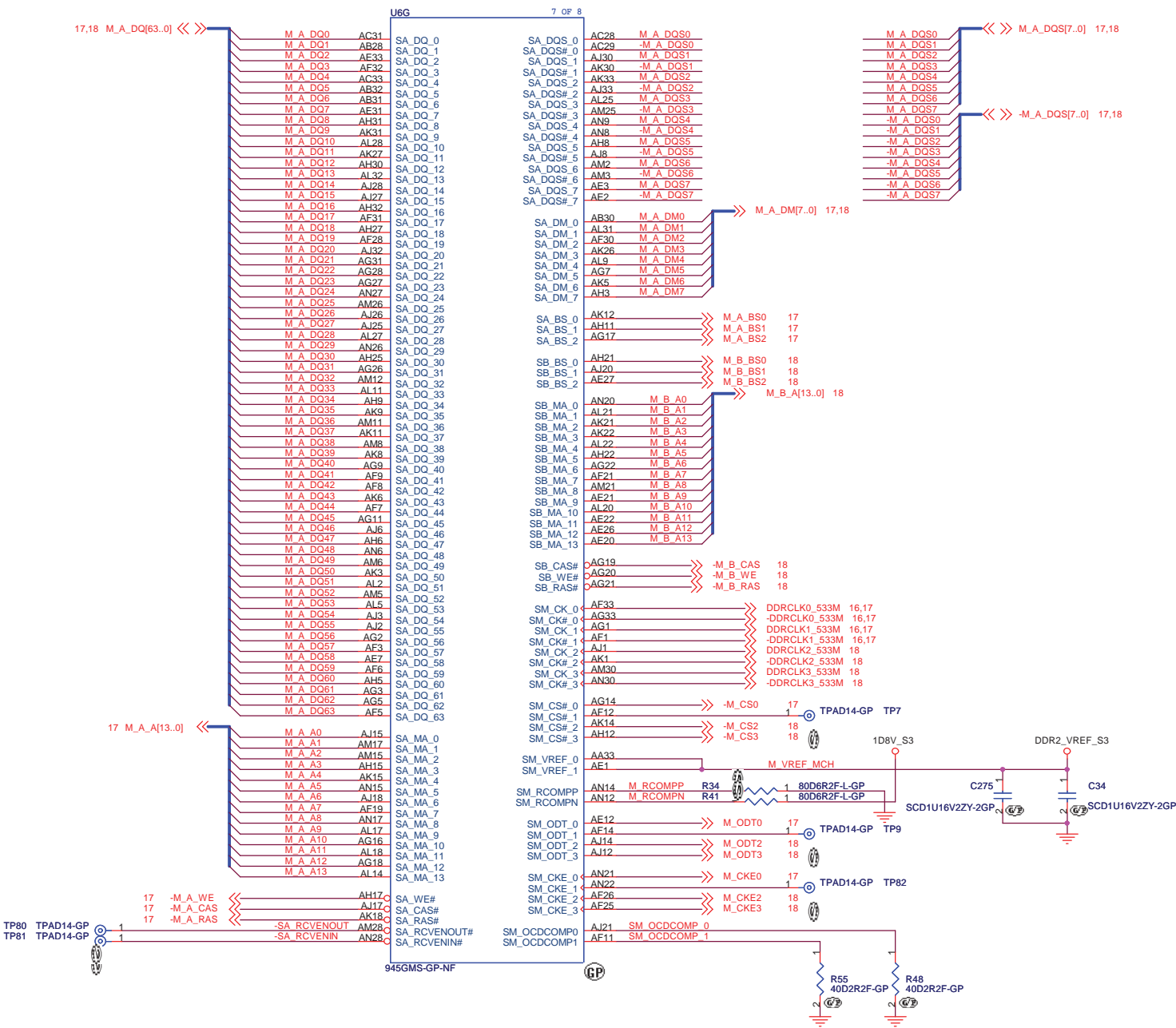
Rev
SB

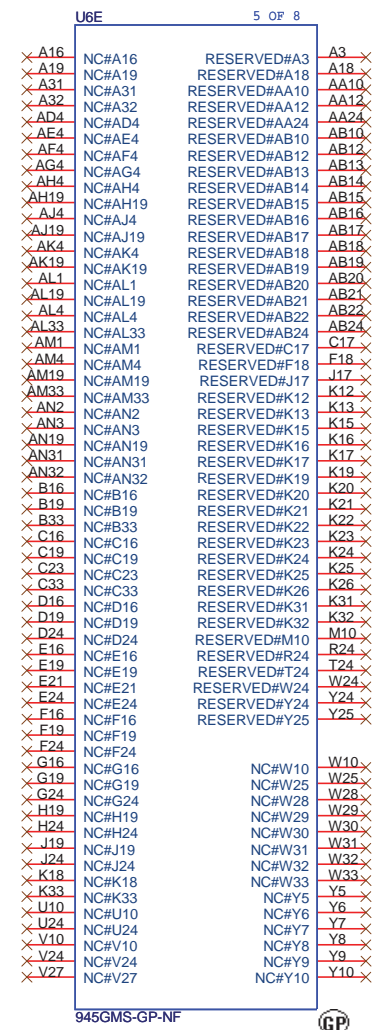
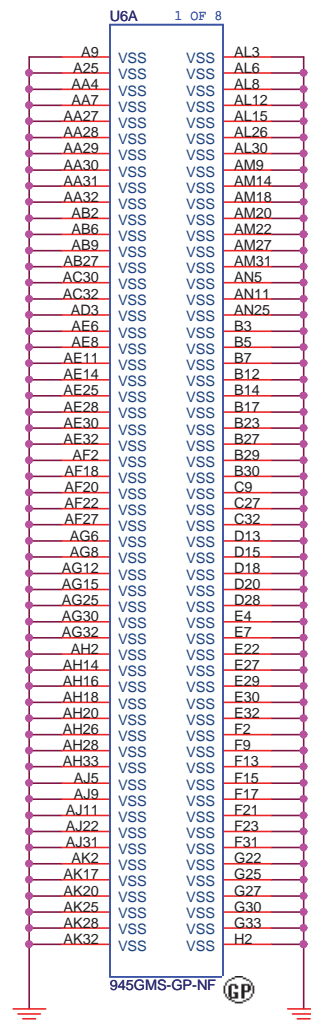
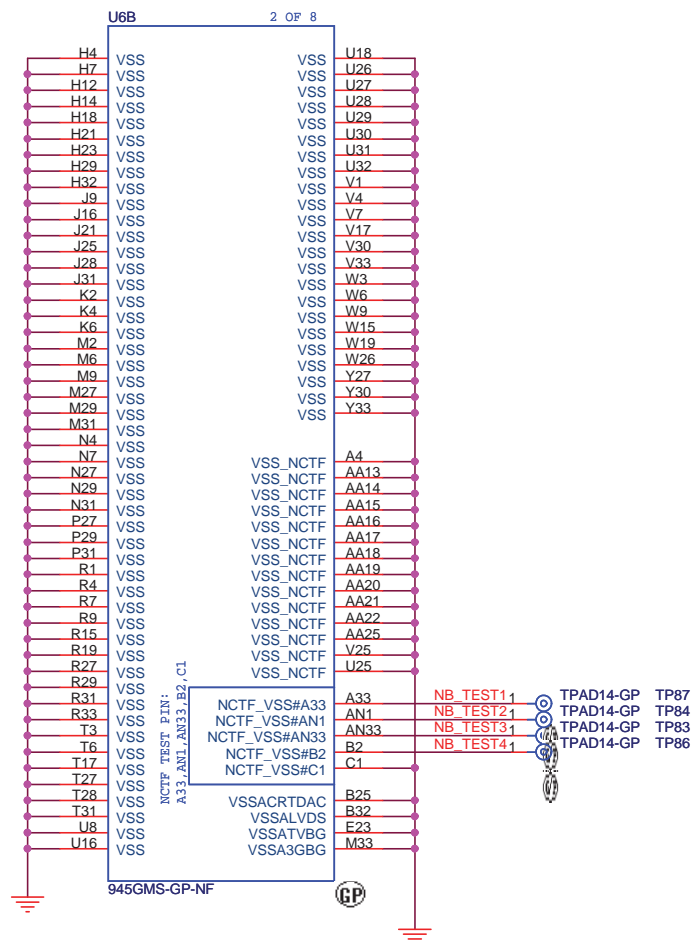
Date: Thursday, January 15, 2009

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41







<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CALISTOGA(6/6):GND

Size	
Cust	

Document Number

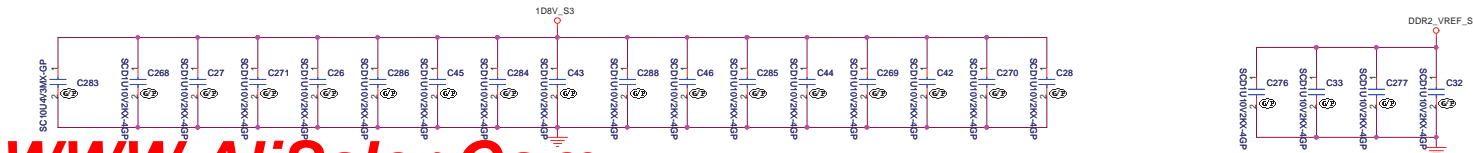
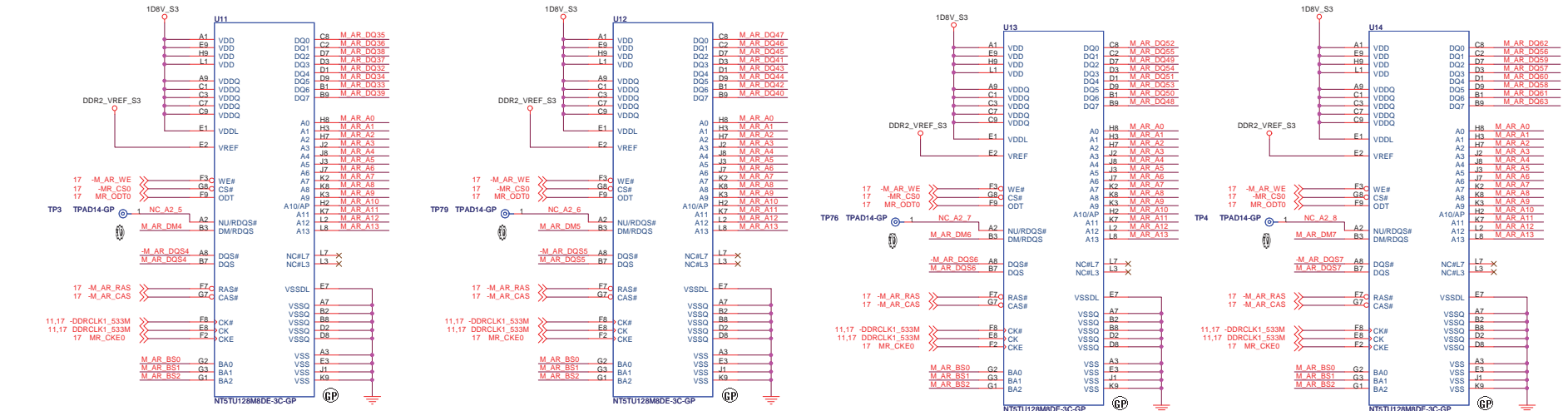
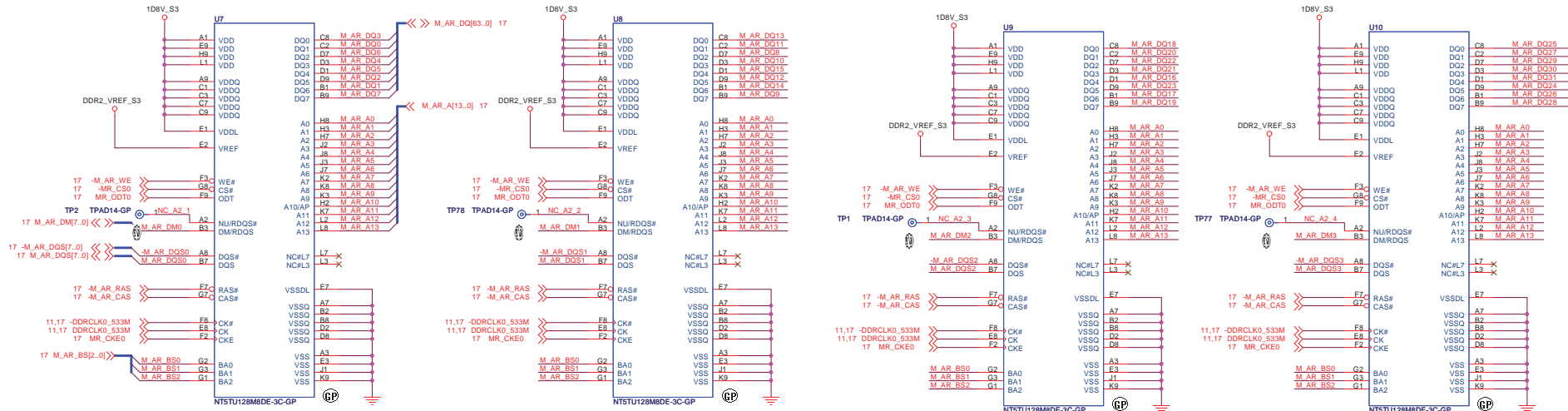
LS20

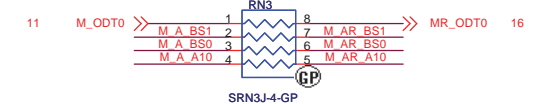
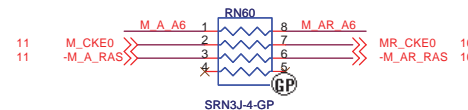
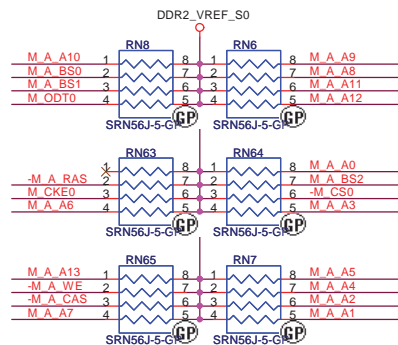
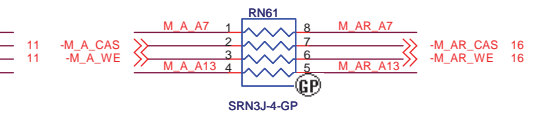
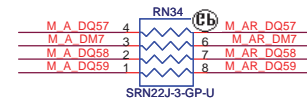
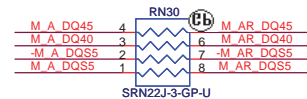
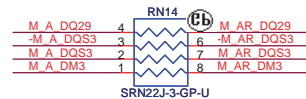
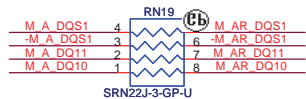
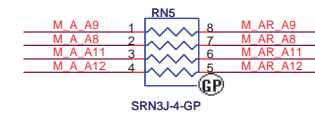
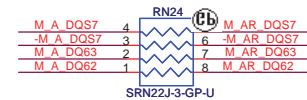
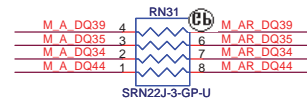
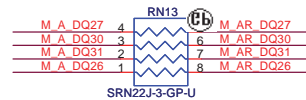
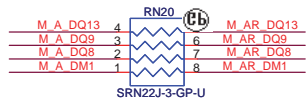
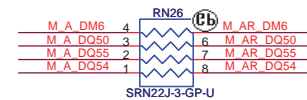
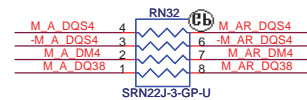
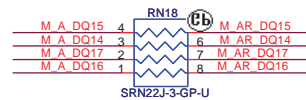
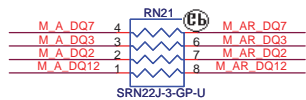
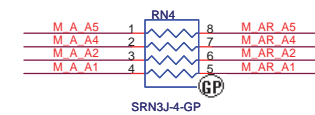
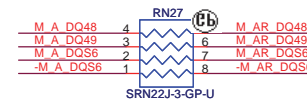
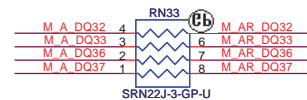
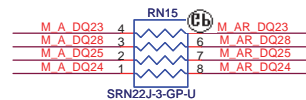
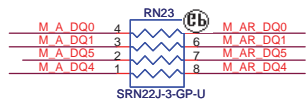
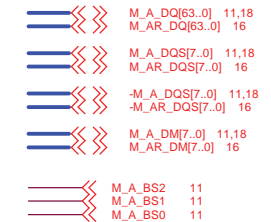
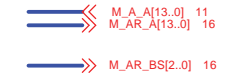
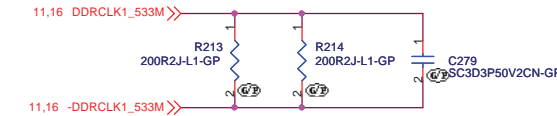
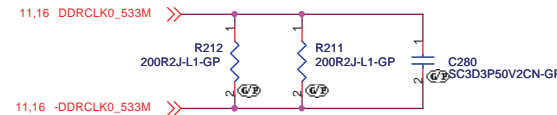
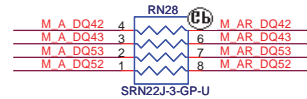
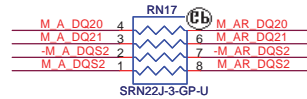
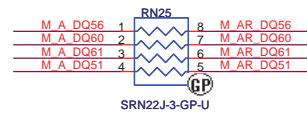
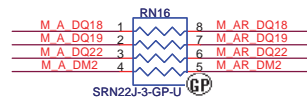
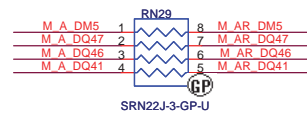
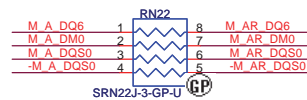
Rev	SB
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On-board DDR2 Memory





<Variant Name>

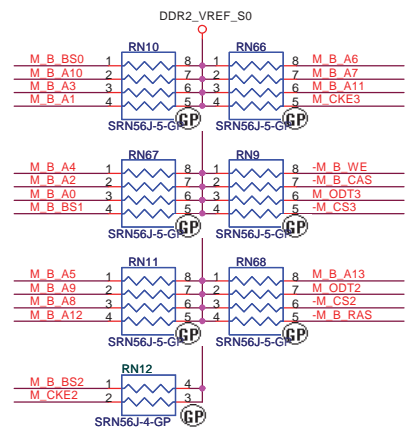
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR-2 On Board(Resistors)**

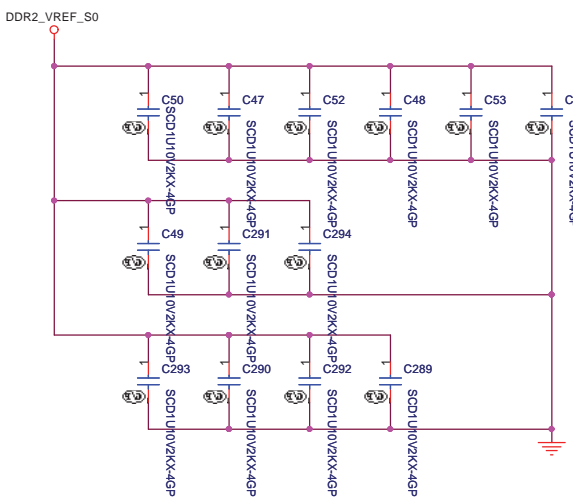
Size A3	Document Number	Rev SB
---------	-----------------	--------

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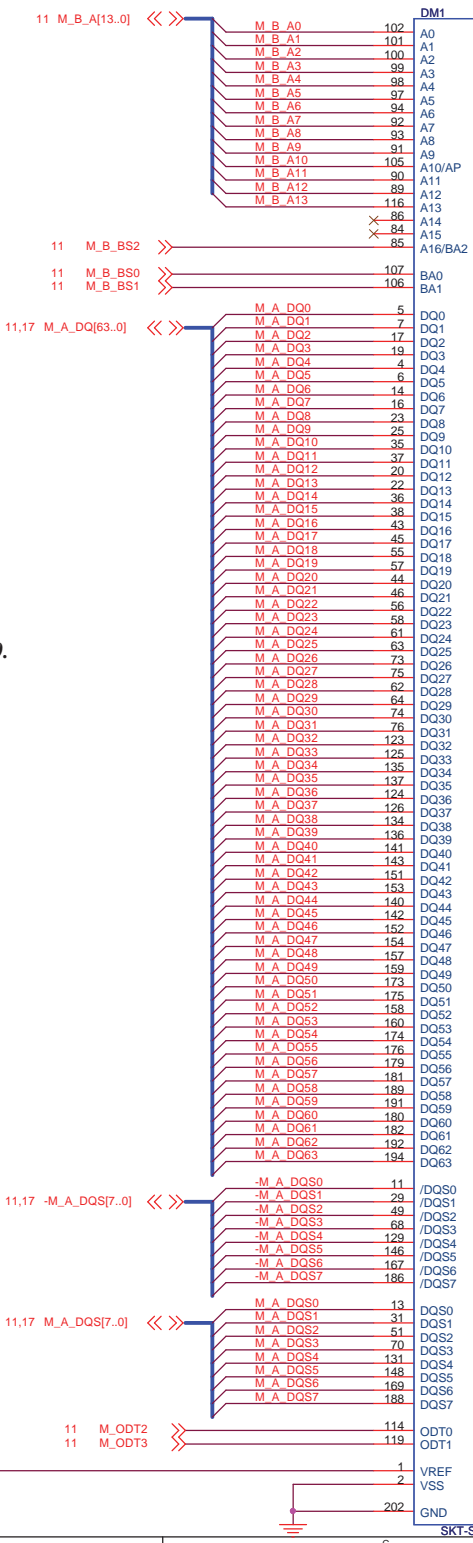
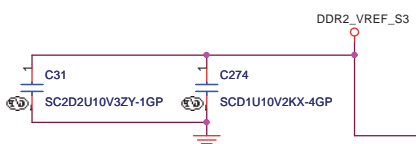
CHANNEL A PARALLEL TERMINATION



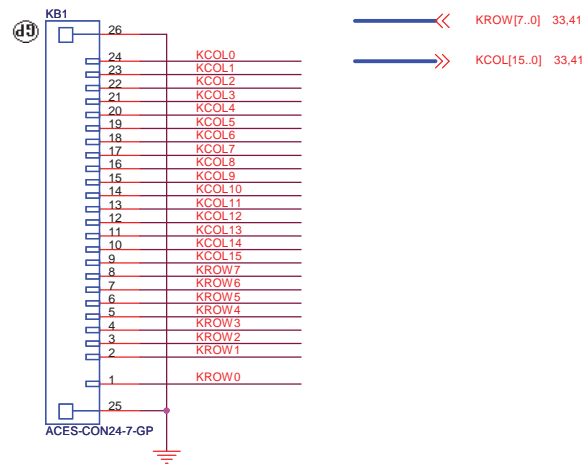
PLACE 1 CAP FOR EVERY 2 BITS TERMINATION TO DDR2_VREF_S0.



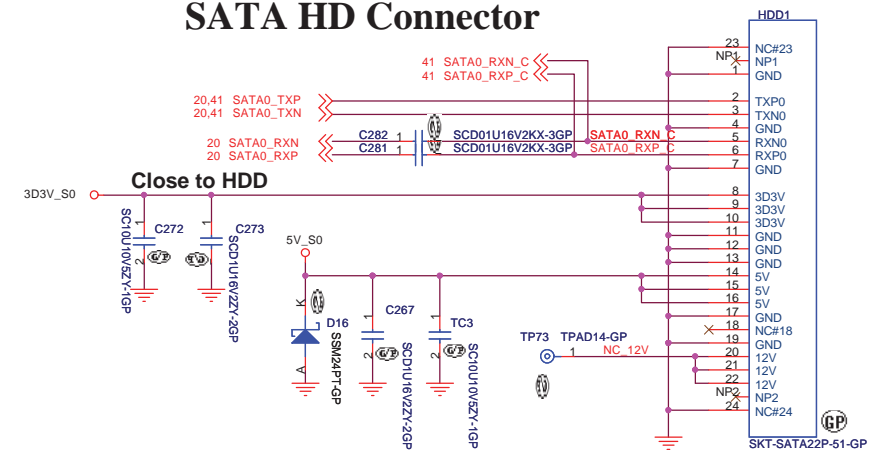
DDR SLOT2 RELATED CAPS ARE REMOVED!



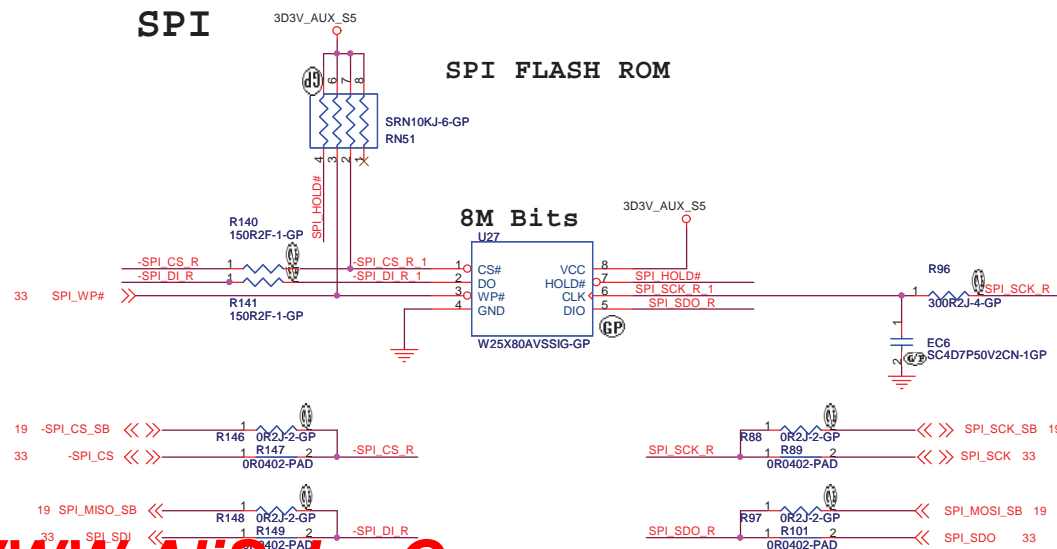
Internal KeyBoard Connector



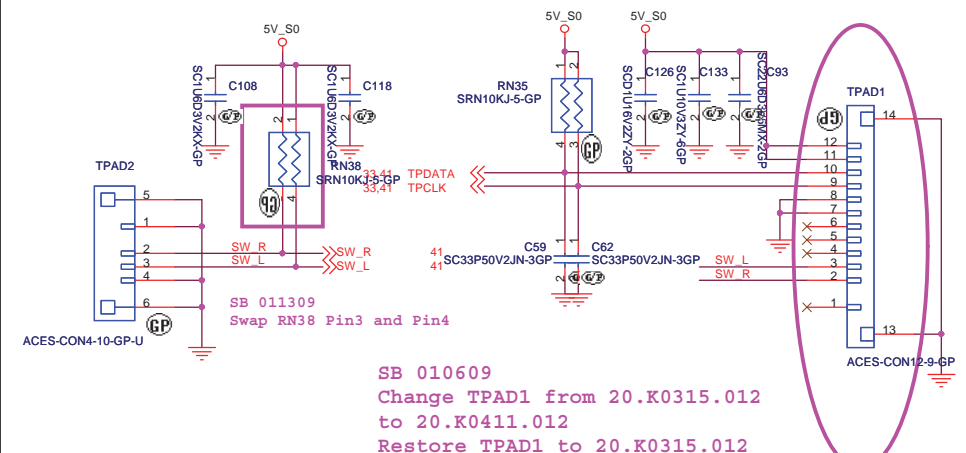
SATA HD Connector



SPI



TouchPad Connector



<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD /KeyBoard / FWH / TouchPad
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Size A3	Document Number 1 S20	Rev SP
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A vertical bar divided into four segments labeled 1, 2, 3, and 4 from bottom to top. An arrow points from the boundary between segments 2 and 3 to the right.



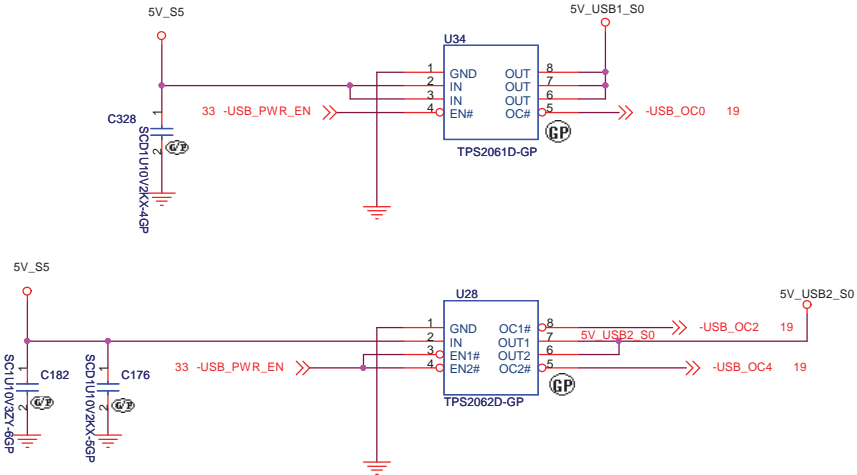
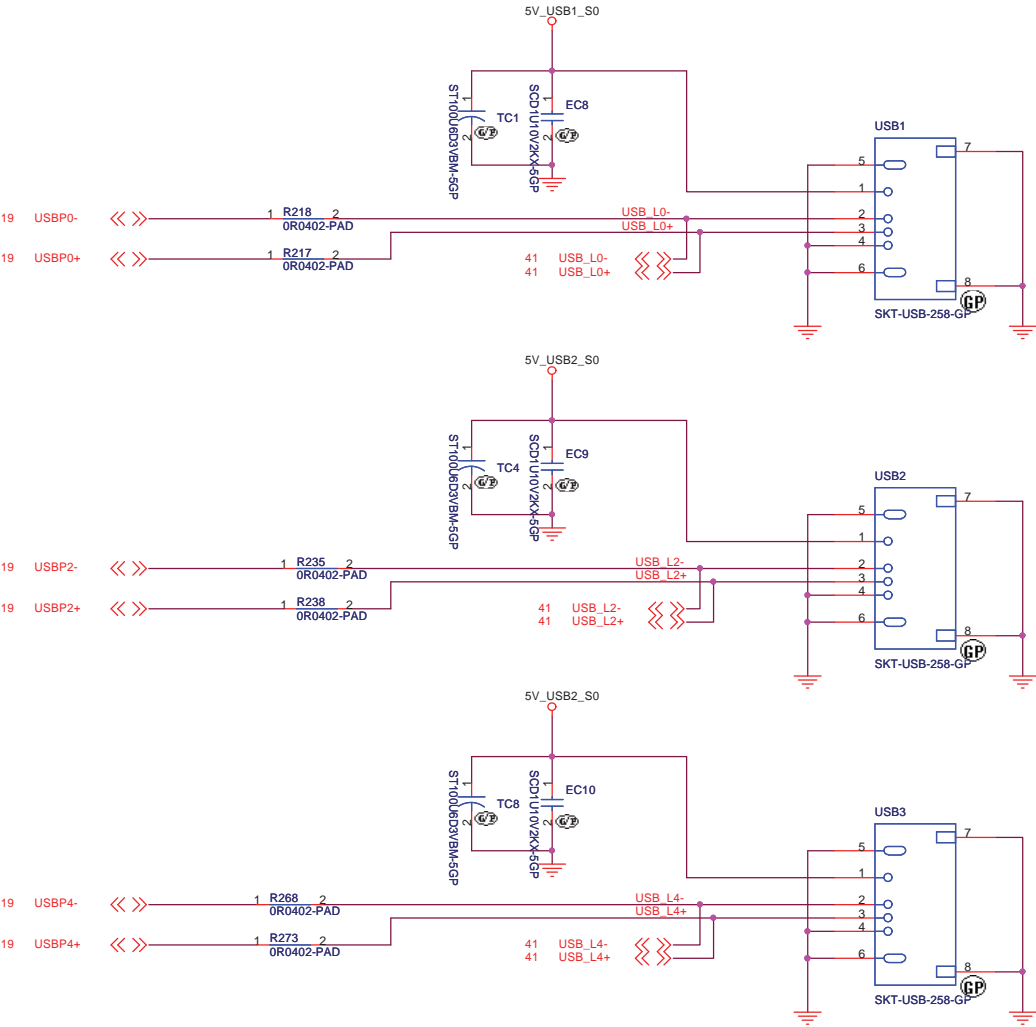
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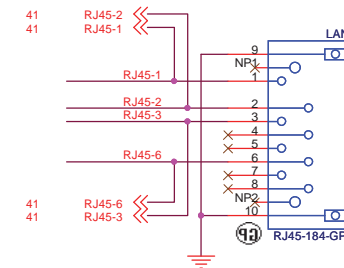
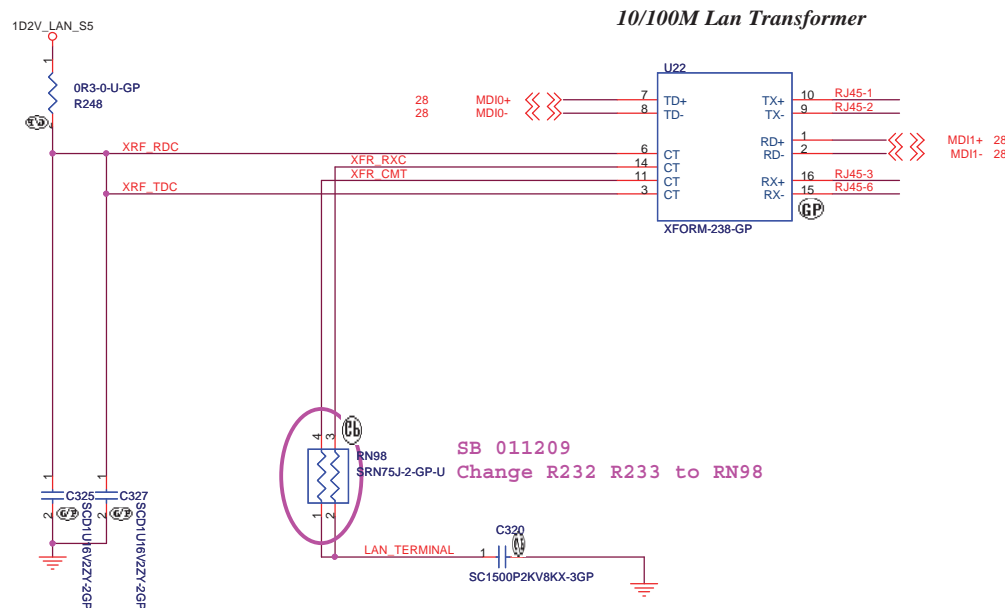
WWW.AliSaler.Com

<Core Design>				1
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title				
CRT Connector				
Size A3	Document Number LS20			Rev SB
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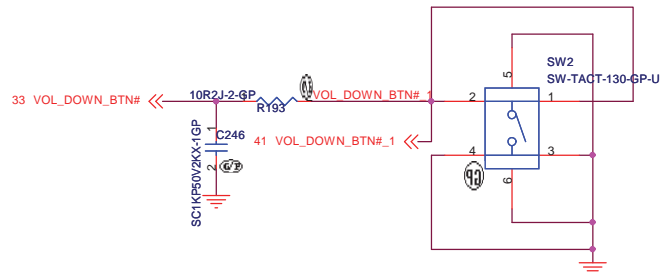
USB x 3 Connector



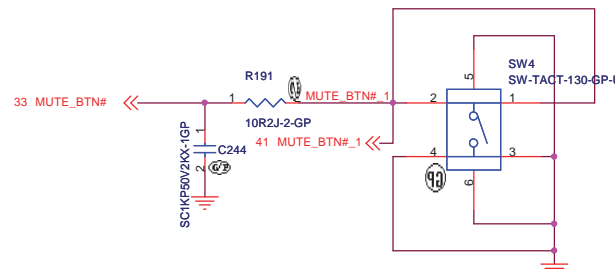
<Variant Name>			
Title			
Size			
Custom			
Date: Thursday, January 15, 2009			
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SB			



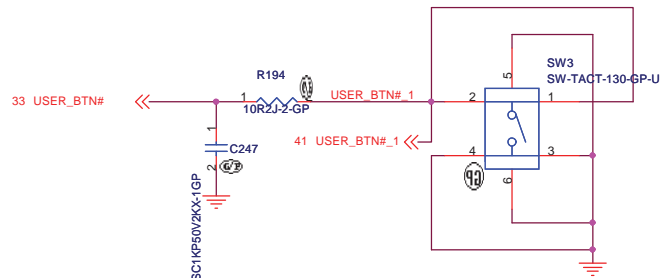
Volume Down Button



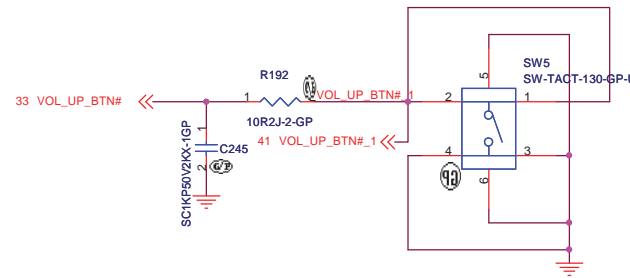
Mute Button



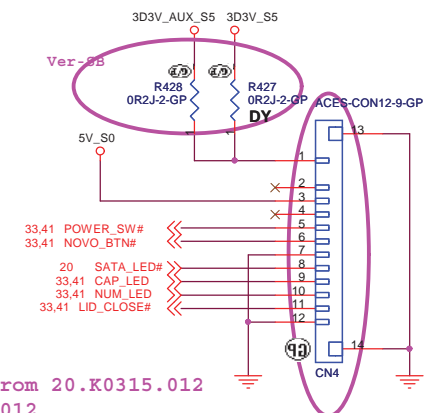
USER Button



Volume Up Button



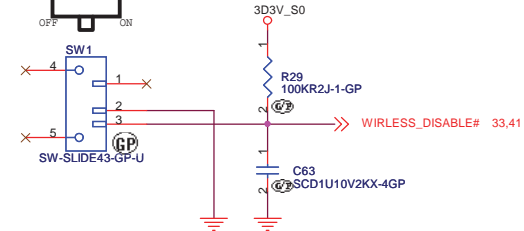
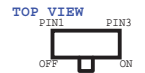
Power Button Board



<Variant Name>

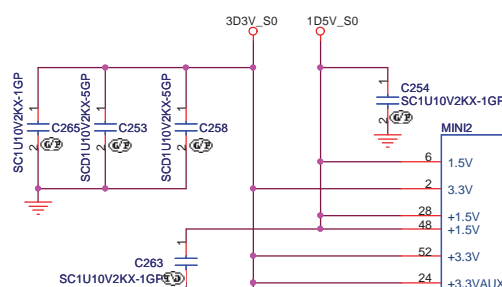
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN connector/ Function Button		
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41 UIM_CLK
41 UIM_RESET
41 UIM_PWR
41 UIM_VPP
41 UIM_DATA

19 USBP5-
19 USBP5+



Ver-SB: Remove Q32 part

FOR DEBUG

33 E51_RXD
33 E51_TXD

FOR DEBUG

Change R208 from DY to ASM

Change R208 from DY to ASM

Ver-SB: Remove Q28 Part

SB 010709

ADD R431

SB 011209

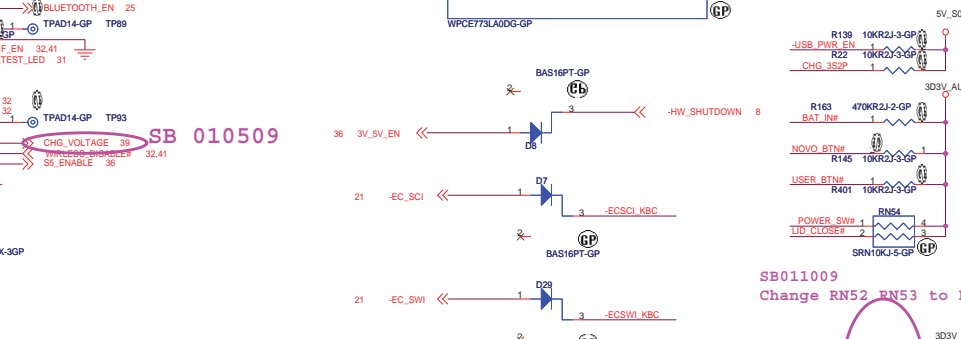
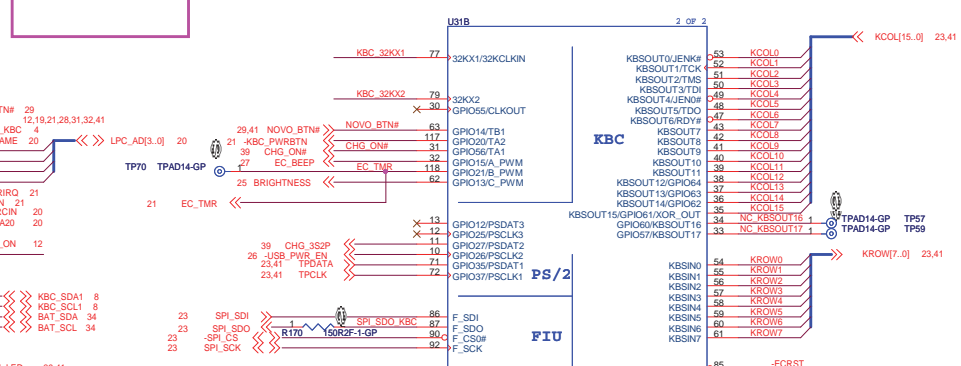
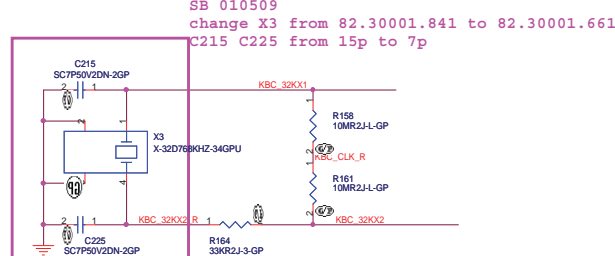
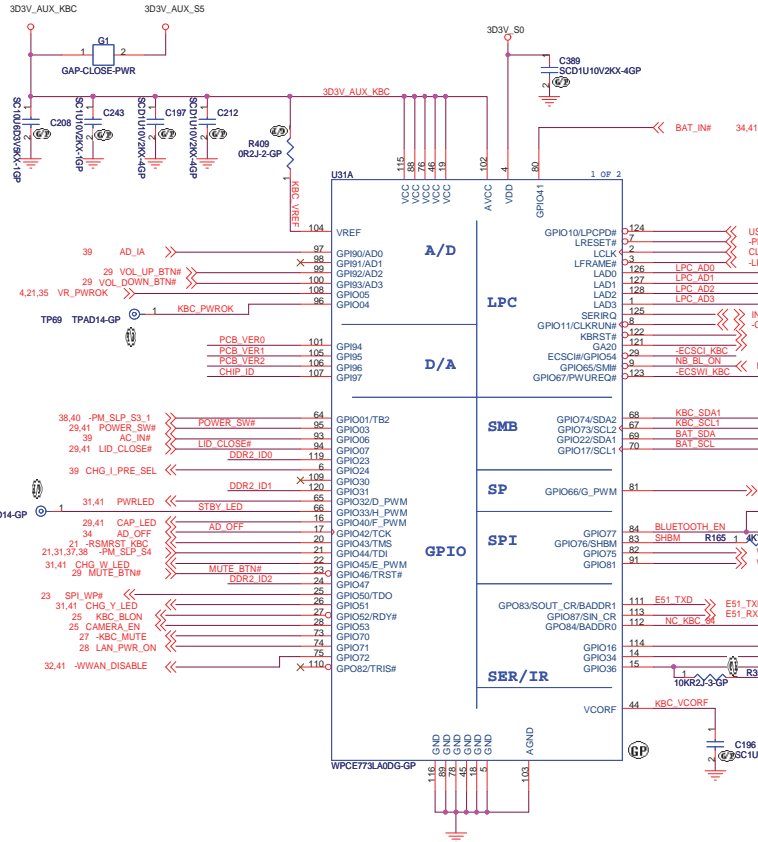
Change R431 to 33 ohm

SB 010609

Change MINI2 from 62.10043.161 to 20.F1107.052

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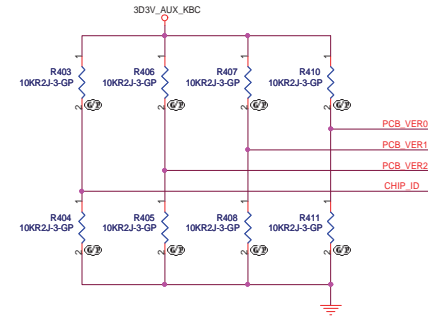
MINI CARD SLOT 1&2		
Size A3	Document Number	Rev SB
LS20		
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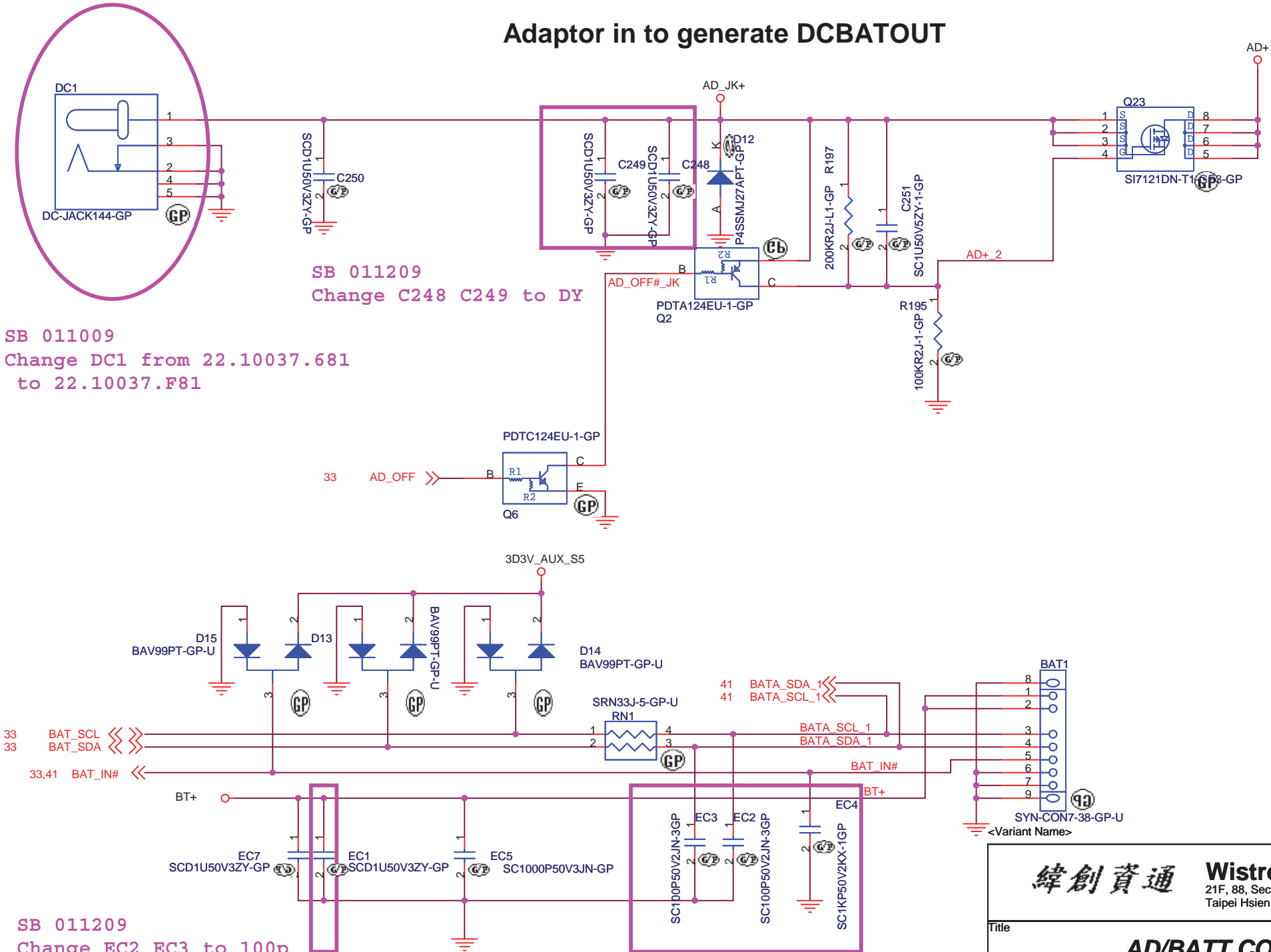
Planar ID	[2, 1, 0]
SA:	0, 0, 0
SB:	0, 0, 1
SC:	0, 1, 0
-1:	0, 1, 1

CHIP_ID	GPI[97]
VIA	0
Intel	1

KBC GPIn	47	31	23		
DDR2_IDn	2	1	0	Vendor Part No.	Size
	0	0	0	HY5PS1G1631CFR-Y5	1G
	0	0	1	NT5TU128M8DE-ACI	1G
	0	1	0	MT47H128M8HQ-3-G	1G



Adaptor in to generate DCBATOUT



緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size
A4

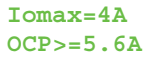
Document Number

LS20

Rev
SB

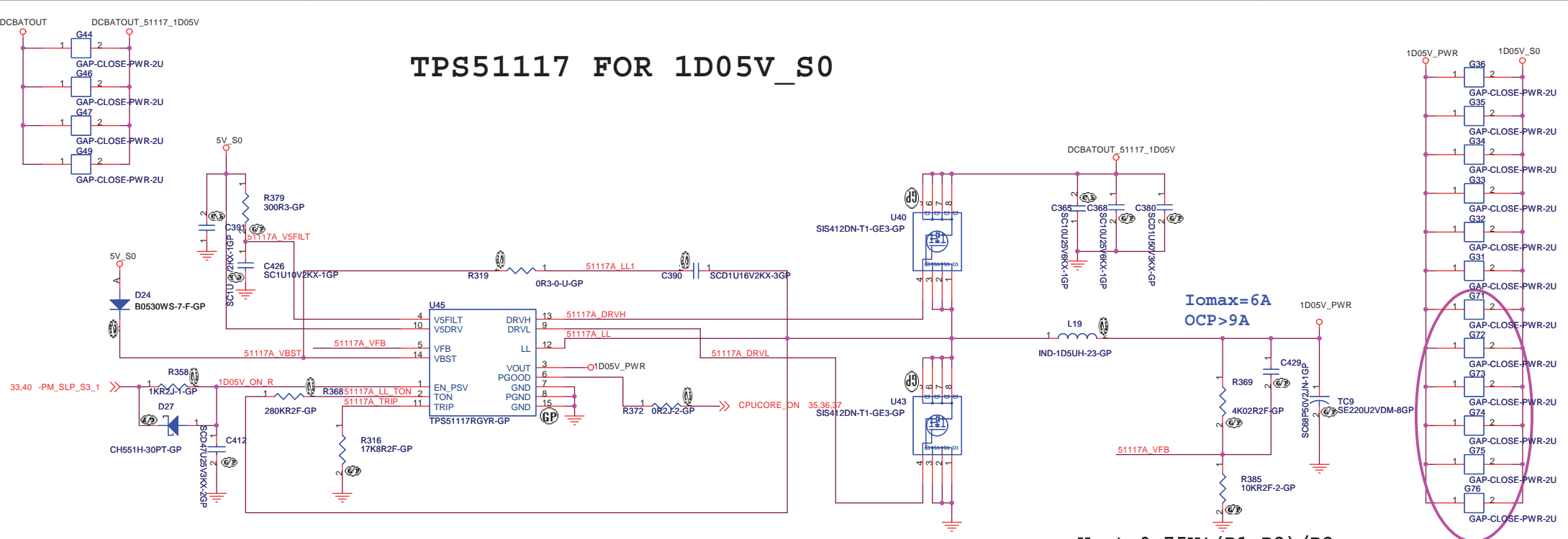
Date: Thursday, January 15, 2009

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[illegible]

TPS51117 FOR 1D05V_S0



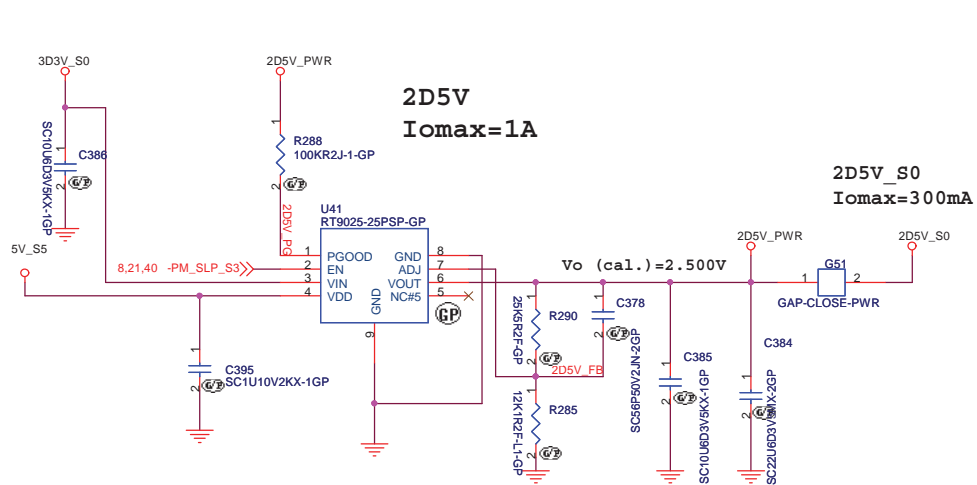
$$V_{out} = 0.75V * (R1 + R2) / R2$$

SB011009

ADD G71 G72 G73 G74 G75 G76

2D5V
Iomax=1A

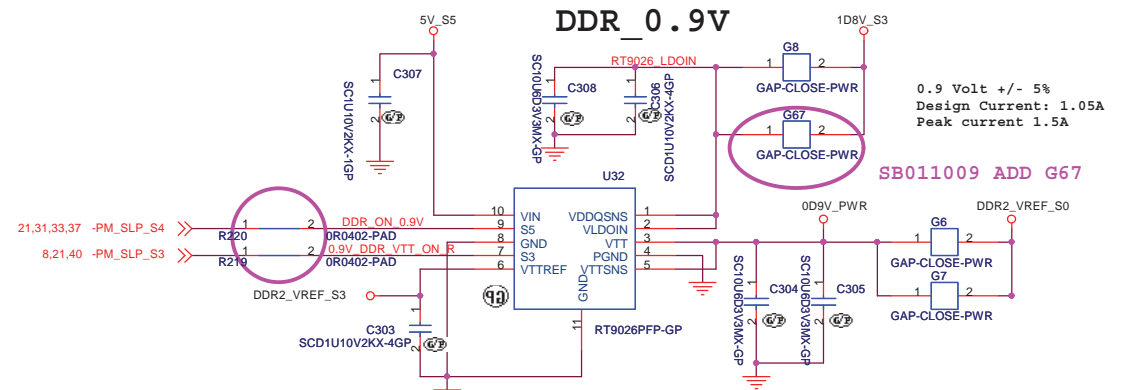
2D5V_S0
Iomax=300mA



$$R_h/R_l = (V_{out}/0.8) - 1$$

DDR_0.9V

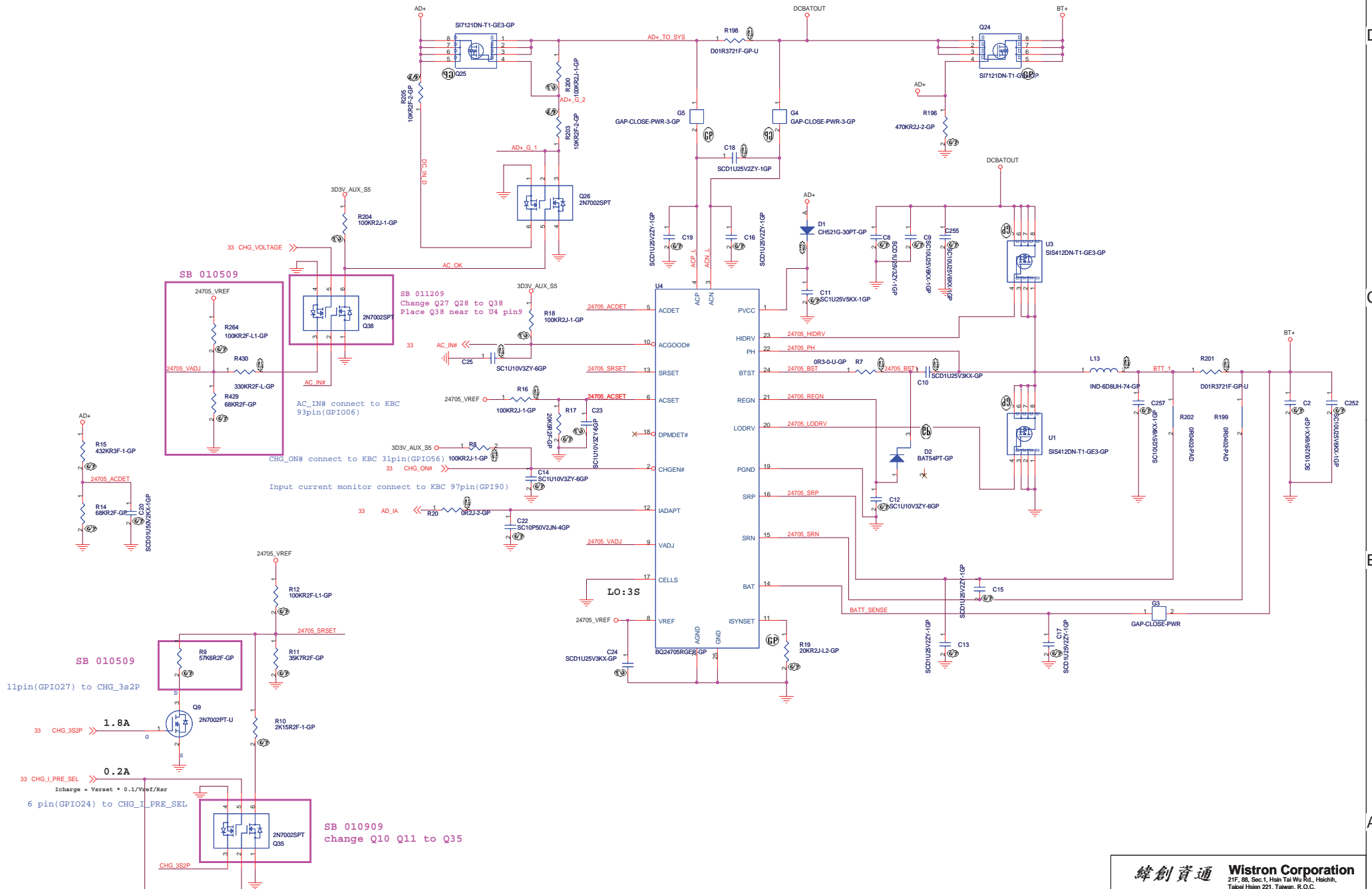
0.9 Volt +/- 5%
Design Current: 1.05A
Peak current 1.5A



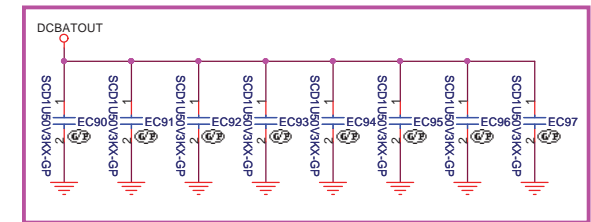
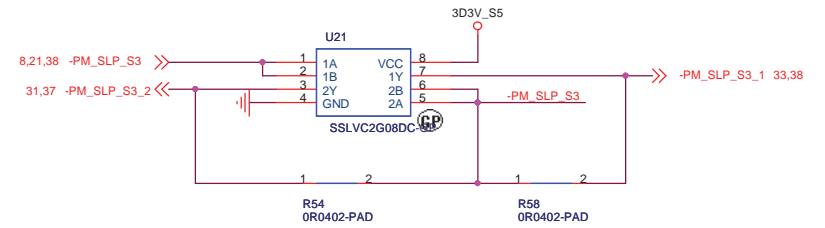
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
TPS51117_1D05V/0D9V/2D5V			
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CHARGER



WWW.AliSaler.Com



H19 HOLE H2 HOLE H21 HOLE H22 HOLE H23 HOLE H24 HOLE H25 HOLE H28 HOLE H30 HOLE H33 HOLE H35 HOLE H36 HOLE H37 HOLE H39 HOLE H56 HOLE H57 HOLE H58 HOLE

H100 HOLE H101 HOLE H102 HOLE H103 HOLE H104 HOLE H105 HOLE H106 HOLE H107 HOLE

H1 H101 ST75C296H3-GP H20 ST75C296H3-GP

H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H15 H16

HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF HOLE315X316R01-S1-GF

K8 K9 K10 K11 K12 K13 K14 K15 K16

SPRING-24-GP SPRING-24-GP SPRING-24-GP SPRING-24-GP SPRING-24-GP

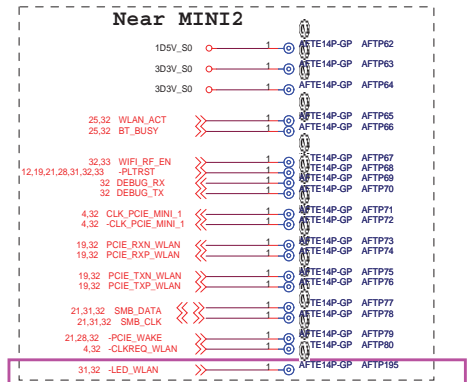
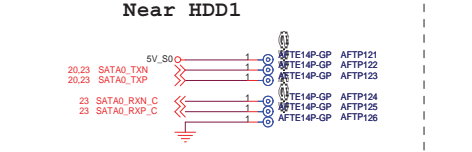
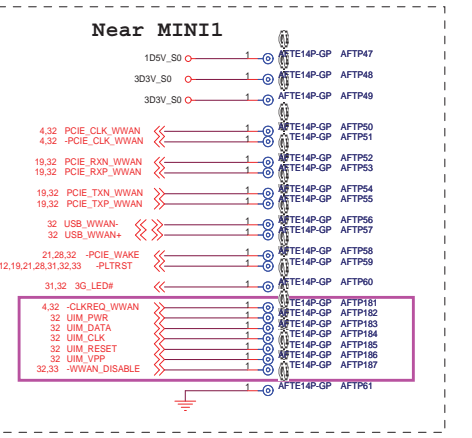
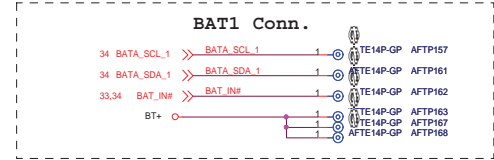
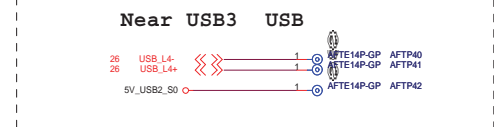
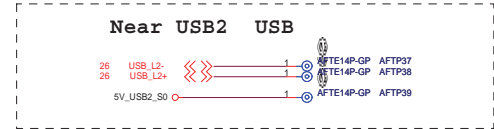
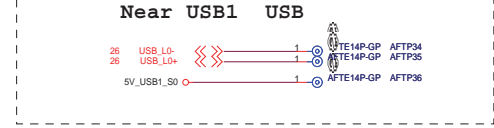
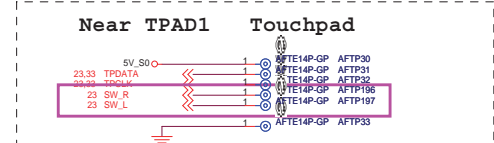
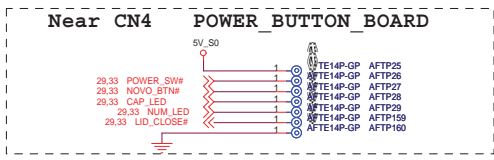
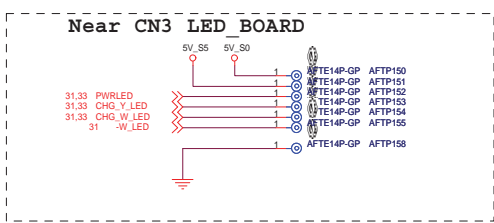
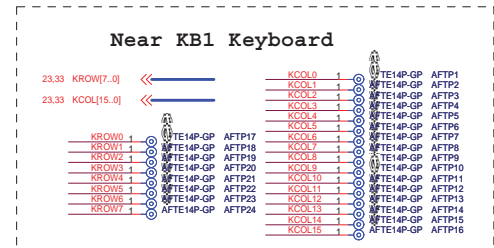
SB 010909
Delete H31 H34

SB 010509
change K4 K5 K6 K7 to 34.45T31.001
Remove K1 K2 K3

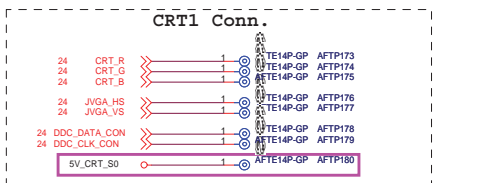
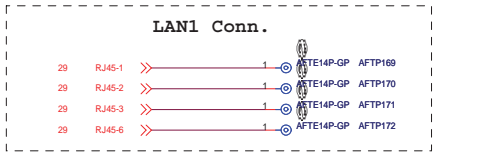
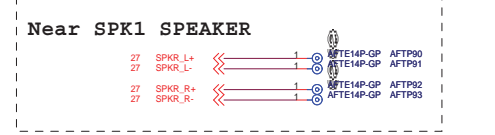
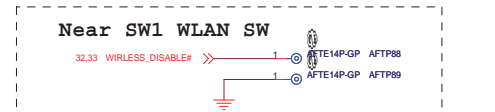
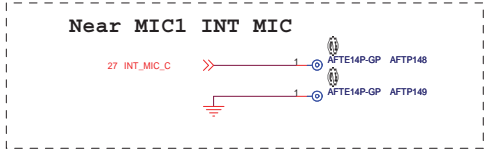
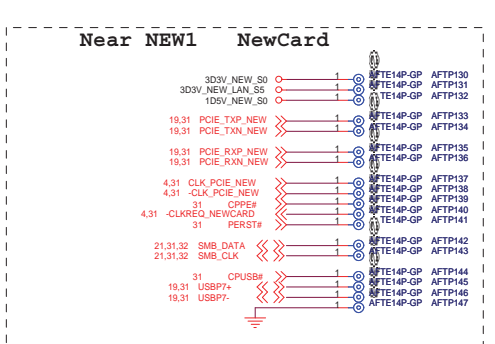
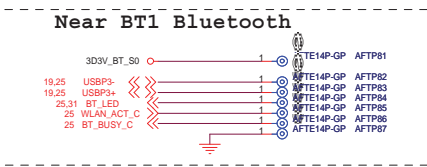
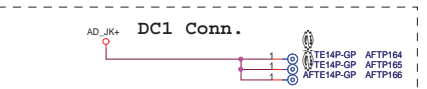
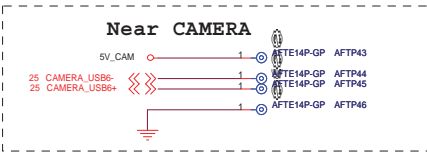
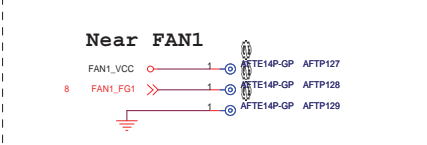
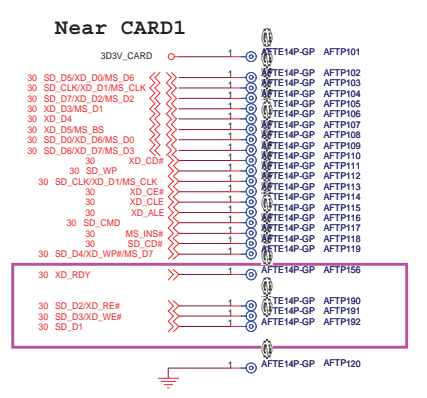
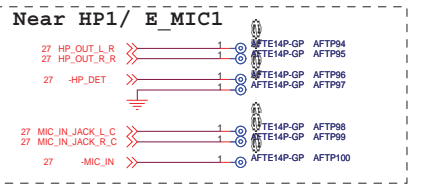
(34.4CK03.001) H56,H57,H58
(34.4CK01.001) H1
(34.4CK02.001) H2
(34.4CK05.001) H21
(34.4CK04.001) H20

SB 010509
Change H2 from
to ZZ.0HOLE.X
Change H21 from
to ZZ.0HOLE.X

SB 011209
ADD K8 to GND for EMC
DY K4 K5 K6 K7 K8



SB011009 ADD



<Variant Name>

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TEST_PAD

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Size: _____
C: _____
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Document Number: **LS20**
Rev: **SB**